

EE574/674 CMOS Digital VLSI Design I

Winter 2008

Abstract

This course is an introduction to CMOS digital IC design. It covers MOS transistor theory and device fabrication, design of CMOS gates including inverters and more complex structures. Various logic design styles are considered such as static CMOS, pass-transistor logic, and dynamic logic. Lab exercises involve the use of industry standard design tools for layout design and simulation.

Lectures

Meeting time: Monday & Wednesday, 7:00pm – 9:00pm.
Room: Paul Clayton Building, Room PC401

Required Text

- *CMOS Digital Integrated Circuits: Analysis and Design (3rd ed.)*, Kang and Leblebici

Suggested Texts

- *Digital Integrated Circuits, A Design Perspective (2nd ed.)*, Rabaey, Chandrakasan, and Nikolic (*Used in the follow up course: EE575/675*)
- *CMOS VLSI Design (3rd ed.)*, Weste and Harris
- *CMOS: Circuit Design, Layout and Simulation (2nd ed.)*, Baker
- *CMOS Logic Circuit Design*, Uyemura
- *Microelectronic Circuit Design (3rd ed.)*, Jaeger

Supplementary Texts

- *Device Physics*

- *Solid-State Electronic Devices*, Ben G. Streetman
- *Modern VLSI Devices*, Taur
- *Operation And Modeling Of The MOS Transistor*, Tsividis

- *Analog CMOS Circuits*

- *Design Of Analog Integrated Circuits*, Razavi
- *CMOS Analog Circuit Design*, Allen

- *VLSI Processing*

- *Fundamentals of Semiconductor Processing*, Sze
- *Introduction To Microelectronic Fabrication*, Jaeger
- *The Science And Engineering Of Microelectronic Fabrication*, Campbell

Instructor

- Kartik Raol
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- Office hours: before and after class, or by appointment.

Overview of topics:

- (6 lectures) Operation of P/N junctions and diodes. Understanding of MOS capacitor and NMOS and PMOS transistors. Derivation of I/V characteristics, threshold voltage, and intrinsic capacitances. Overview of semiconductor device fabrication and modeling using Spice.
- (5 lectures) Overview of inverter types, including pseudo-NMOS, CMOS, etc. Understanding of inverter noise margins, power consumption, and propagation delays. Introduction to interconnect design, parasitics, Elmore delay, buffer insertion, and power and noise characteristics of long interconnects.
- (4 lectures) Understanding of more complex CMOS gates and CMOS design styles, including layout methodology. Includes determination of gate delay using effective pull-up and pull-down strengths, and effect of device sizing and input ordering.
- (4 lectures) Other logic styles including transmission gate logic and dynamic logic. Sequential circuits and basic clocking. Datapath blocks such as adders and multiplier circuits.

Grading:

- There will be a midterm and a final exam, each counts for 25% of the final grade
- There will be ~5 homeworks and in-class quizzes, total 30% and some optional homeworks for extra credit
- Final project counts for 20% of grade
- These are guidelines only! I reserve the right to change the grading at any time.

Class Syllabus (subject to change) March 17 and 19 are regular lecture days to make up for 2 classes lost due to holidays. Final exam on Friday March 21 (extra lecture day)

#	Date	Lecture Topic	Book Section
1	Mon Jan 7	Course overview Atomic models, bonding types Intrinsic semiconductors, band diagrams	Ch. 1
2	Wed Jan 9	Extrinsic doping Electron drift and diffusion PN junction: band diagram & biasing	3.1
3	Mon Jan 14	MOS capacitor & energy band diagram Inversion	3.2-3.3
4	Wed Jan 16	MOS transistor Threshold voltage	3.3
	Mon Jan 21	Martin Luther King Day – No Class (holiday)	
5	Wed Jan 23	MOS I/V Equations MOS capacitances Short-channel effects Transistor leakage	3.4-3.6

6	Mon Jan 28	MOS scaling Spice simulation IC Fabrication	2.1-2.5 Ch. 4
7	Wed Jan 30	Inverter characteristics Resistive-load inverter Pseudo-NMOS & depletion inverter	5.1-5.3
8	Mon Feb 4	CMOS inverter Inverter capacitances	5.4, 6.1
9	Wed Feb 6	CMOS inverter delay & power Buffer design	6.2-6.4, 6.7, Appendix
10	Mon Feb 11	Interconnect Presentation	6.5-6.6 – Extra
11	Wed Feb 13	Switch-level models Review for midterm	
	Mon Feb 18	President's Day – No class (Holiday)	
12	Wed Feb 20	Midterm: Lectures 1 – 10	
13	Mon Feb 25	Static CMOS gates Complex gate design	7.3-7.4
14	Wed Feb 27	Transistor sizing Layout design	7.4
15	Mon Feb 3	CMOS gate capacitances CMOS design guidelines Pseudo-NMOS logic	7.3-7.4 11.4-11.5
16	Wed Mar 5	Transmission gate logic	7.5
17	Mon Mar 10	Dynamic Logic Domino & Zipper logic	9.5-9.6
18	Wed Mar 12	Latches & Sequential Elements	8.3-8.5
19	Mon Mar 17	Adders	9.6
20	Wed Mar 19	Other datapath blocks Final Exam review	
21	Fri Mar 21	Final exam: Lectures 11 – 19 (Extra Class)	